Remarks

I. The Rejections Based on 35 U.S.C. § 103

Claims 1, 2, 8, 9, and 20-22 have been rejected under 35 U.S.C. § 103 as obvious from Chen U.S. patent 6,041,090 ("Chen") in view of To et al. U.S. patent application publication 2003/0167417 ("To"). These rejections are respectfully traversed.

A. Claims 1 and 2

Claim 1 specifies, inter alia, "circuitry for selecting two, phase-adjacent ones of the clock signals that currently have transitions on respective opposite sides of transitions in a serial data signal." It is easy to see that To shows nothing like this because To only mentions selecting and working with clock signals that are within a data sample. For example, in connection with FIG. 9B To only mentions the possibility of selecting and subsequently working with either (1) clock signal pair s_clk1 and s_clk4, or (2) clock signal pair s_clk2 and s_clk3. (See, for example, To paragraph [0044] which describes the alternative of selecting s_clk1 and s_clk4; while To paragraph [0045] describes the alternative of selecting s_clk2 and s_clk3.) To wants to select s_clk signals that are within a data sample because To is then going to interpolate between the selected s_clk signals to

produce a "synthesized clock" signal having transitions near the midpoint of the data samples. Transitions in this synthesized clock signal are used for sampling the data samples.

Applicants' apparatus as defined in claim 1 works altogether differently than what is shown in To. Thus, for example, applicants' apparatus selects two phase-adjacent clock signals that are on respective opposite sides of transitions in the data signal, not on the same side of such data signal transitions as in To. To is therefore fundamentally irrelevant to applicants' claim 1, and To accordingly adds nothing to Chen that can be said to render claim 1 obvious.

Chen is also fundamentally different from applicants' invention as defined in claim 1. The Chen system is constructed so that it is always known in advance that one particular clock signal is best for sampling certain selected ones of the data bits coming through that system. For example, in the illustrative embodiment to which Chen gives most attention, it is known from the design of the system that the CLOCK1 signal (FIG. 3) is always going to be the best signal for sampling data bits 0, 0 + 5, 0 + 10, etc. The CLOCK1 signal is therefore always used for sampling those data bits. To make sure

that the CLOCK1 signal does not drift unacceptably from the center of bits 0, 0 + 5, 0 + 10, etc., another clock signal (e.g., CLOCK4), which it is known should have transitions synchronized with transitions in the data signal, is used in phase locked loop circuitry in which the phases of the CLOCK4 and data signals are compared. This enables the timing of the CLOCK1 signal to be adjusted, if necessary, to keep transitions in CLOCK1 centered on data bits 0, 0 + 5, 0 + 10, etc. (Indeed, any or all of the CLOCK signals can be used in this way; and the result is that all of the clock signal transitions are kept centered in the respective data bits that each clock signal is used to sample.)

The point of the preceding summary of Chen is to demonstrate that Chen's circuitry performs no clock signal selection. The clock signals that Chen uses for various purposes are the result of the design of Chen's circuitry, not the result of any signal selection operation of Chen's circuitry. Chen therefore shows nothing comparable to applicants' "circuitry for selecting two, phase-adjacent ones of the clock signals that currently have transitions on respective opposite sides of transitions in a serial data signal signal."

The foregoing demonstrates that neither Chen nor To shows or suggests at least one of the elements (i.e., the "circuitry for selecting") specified by applicants in claim 1. Claim 1 and its dependent claim 2 are therefore not obvious from Chen and To, and these claims should accordingly be allowed.

B. Claims 8 and 9

Claim 8 refers to "changing the selected phase-adjacent clock signals until the phases of the selected two phase-adjacent clock signals are predominantly on respective opposite sides of the phase of the serial data signal." Applicants' invention as defined in claim 8 thus includes finding two phase-adjacent clock signals having phases that are on respective opposite sides of the phase of the data signal. To does not do anything like this because To only works with clock signals having phases that are on the same side of the phase of the data signal. (See again the above discussion of how To works with either signals s_clk1 and s_clk4 or with signals s_clk2 and s_clk3, all of which have phases on the same side of the phase of the data sample in To FIG. 9B.)

Chen also does nothing like what is quoted from claim 8 above because Chen does no "changing" of the clock signals used for any purpose. The Chen circuitry is

designed and therefore constructed to always use the same clock signals for the same purposes. For example, the CLOCK1 signal is always used to sample bits 0, 0 + 5, 0 + 10, etc. Similarly, the CLOCK4 signal is always used to test for phase alignment at the ends of data bits 0, 0 + 5, 0 + 10, etc. It is true that Chen says that the circuit can also be constructed to perform one or more other phase alignment tests if desired. For example, such another phase alignment check can be performed by comparing the CLOCK5 signal to the end of bits 1 + 5, 1 + 10, etc. But this is always a matter of how the Chen circuit is constructed to operate. It is not the result of any ability of the Chen circuit itself to change what clock signals it uses for various purposes.

The foregoing demonstrates that nothing like the "changing" step defined by applicants in claim 8 is shown or suggested in either or both of Chen and To. Once again, the Chen circuitry has no ability to change how it uses its various clock signals, and To does not use signals having phases on opposite sides of the phase of the data signal. Claim 8 is therefore not obvious from Chen and To, and claim 8 should therefore be allowed. The same is true for claim 9, which is dependent from claim 8.

C. Claims 20-22

Distinctions of the kinds that are made above for other claims apply again to claim 20. This claim again refers to phases of "two phase-adjacent signals ... on respective opposite sides of the phase of the serial data signal." This (among other differences) distinguishes claim 20 from To, which always works with clock signals, having phases on the same side of the phase of the data signal. Claim 20 also refers to "circuitry ... for controlling the circuitry for controllably selecting to change the selected phase-adjacent clock signals." This distinguishes Chen, which is constructed to always make use of the same clock signals for the same purposes, and which has no ability to select different clock signals for use at different times.

Thus, again, the foregoing demonstrates that claim 20 is not obvious from either or both of Chen and To. Claim 20 is therefore allowable; and the same is true for claims 21 and 22, both of which are dependent from claim 20.

II. The Indication of Allowable Subject Matter

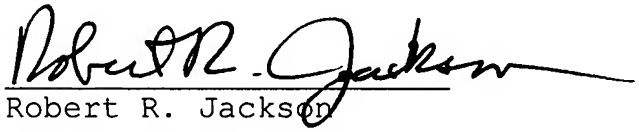
Applicants note with appreciation the indication of allowable subject matter in claims 3-7, 10-19, and 23-34. Because the claims from which these claims depend

have been shown above to be allowable, these claims should now be allowed.

III. Conclusion

The foregoing demonstrates that claims 1-34 are allowable. This application is therefore in condition for allowance. Reconsideration and allowance are accordingly respectfully requested.

Respectfully submitted,



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